Superconducting Microelectronics for Next-Generation Computing

Leonard M. Johnson

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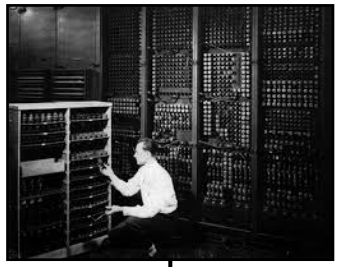
Computing Development Timeline

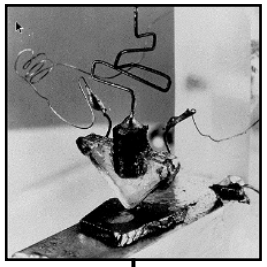
Triode vacuum tube invented

1907

ENIAC



Transistor invented



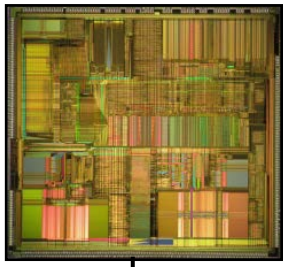
1946

First fully transistor-based computer: TX-0

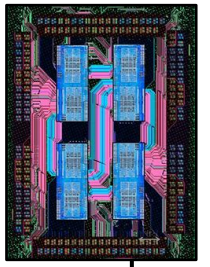
30k transistors: i8088

1971

4.5M transistors: Pentium



19.2B transistors: 32-core Epyc GPU



2017

Vacuum tubes

Discrete transistors

Bipolar transistor integrated circuits

CMOS integrated circuits

*RSFQ: Rapid Single Flux Quantum
**AQFP: Adiabatic Quantum Flux Parametron

Computing Development Timeline

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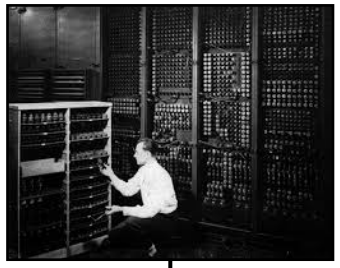

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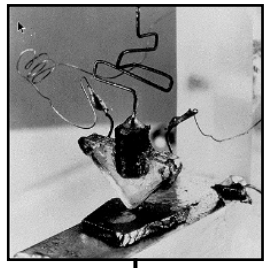

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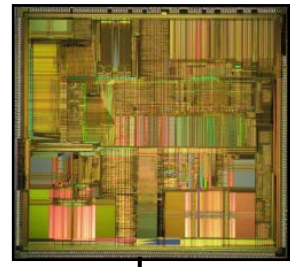

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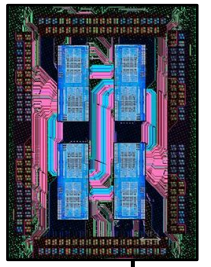
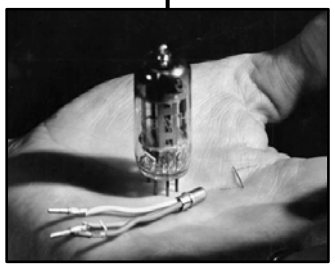
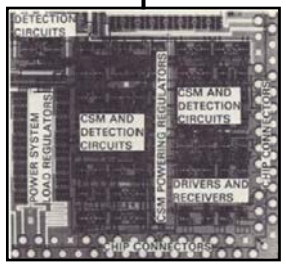


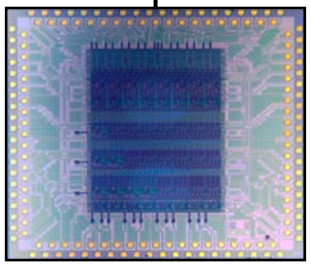
2017



Cryotron

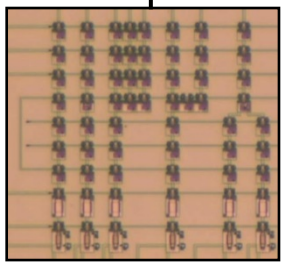


IBM Latching Logic



RSFQ* Circuits

AC-Clocking



AQFP** Circuits

*RSFQ: Rapid Single Flux Quantum
**AQFP: Adiabatic Quantum Flux Parametron

Computing Application Space

Wearables / Implants

Personal Computing

Centralized Computing

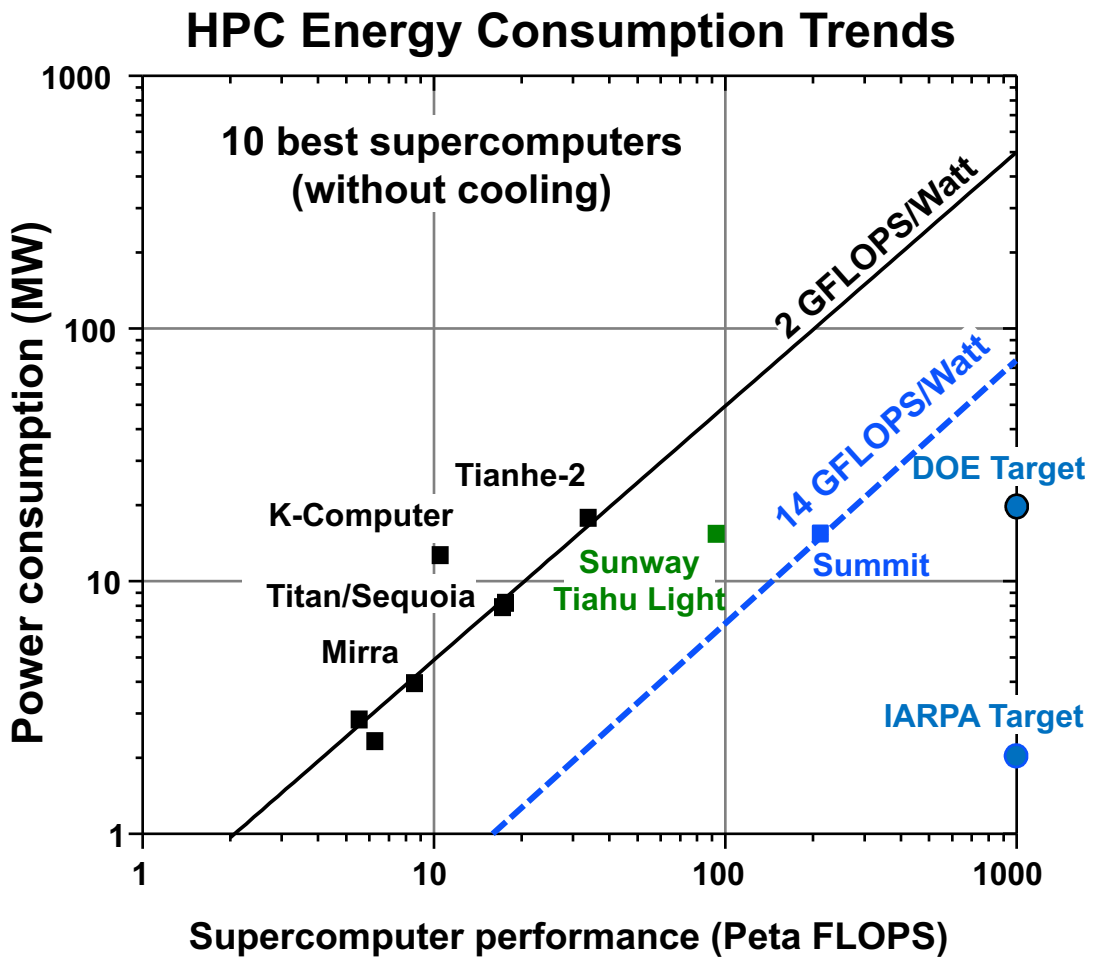
Titan Supercomputer at ORNL

Facebook Data Center

Low Power, Limited Processing ***High Power, Massive Processing***

High Performance Computing (HPC) Energy Consumption Limitations

- **Exascale computer projected to consume ~100 MW with existing approaches**
  - **~1 B kW-h / year**
  - **~$50M / year for electricity**
- **DOE and IARPA charged with realizing aggressive exascale computing power consumption goals**



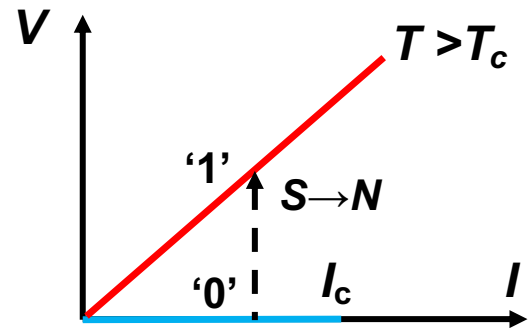
Outline

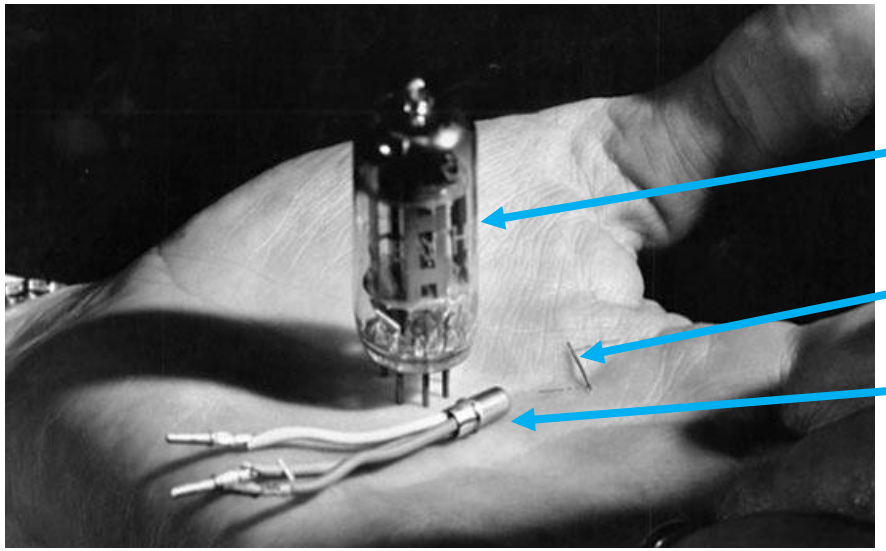
- Introduction to Superconducting Electronics
- Technology Development for Digital Computing
- Additional Applications

First Superconducting Device - Cryotron

- **Superconductivity**
  - Zero dc electric resistance at $T < T_c$
- **Cryotron**
  - Developed at MIT Lincoln Laboratory by Dudley Allen Buck in 1950s
  - Information encoded in the superconducting and normal states of a wire
  - Tantalum wire with wound copper heater
  - Achieved 5-ms switching
  - Spawned research efforts at IBM, RCA, and GE
  - Speed and power never outperformed transistors and efforts were abandoned

I-V Curve for Superconducting Wire

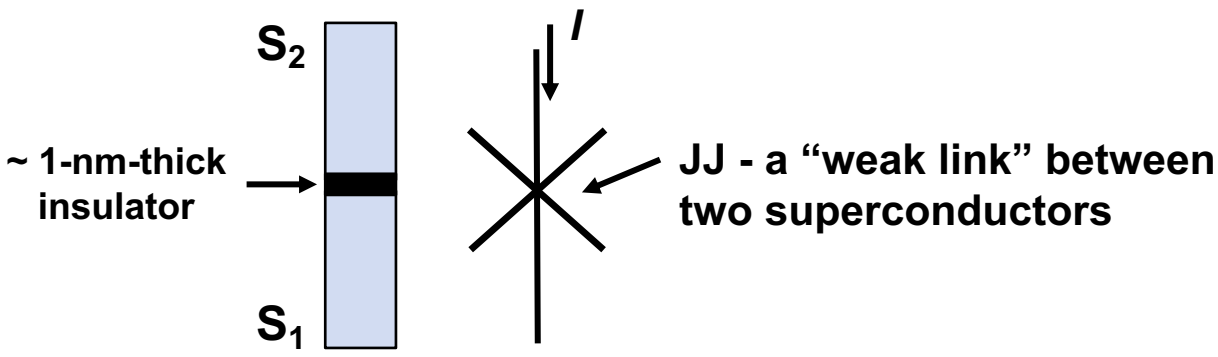




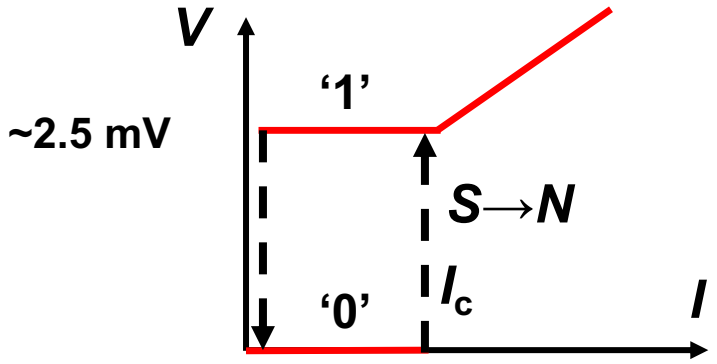
Computing with Superconductivity - Josephson Tunneling Logic

- Josephson tunneling and Josephson junction
  - Superconductor-Insulator-Superconductor
- Josephson Tunneling Logic
  - Information encoded in the normal and superconducting states of the JJ
  - Ultrafast, ~ 1 ps $S \rightarrow N$ switching by current $I > I_c$
  - Slow, ~ 1 ns $N \rightarrow S$ switching back
  - ~100 person effort at IBM from 1970 to 1982
  - No path identified to outperform transistors

Josephson Junction (JJ)



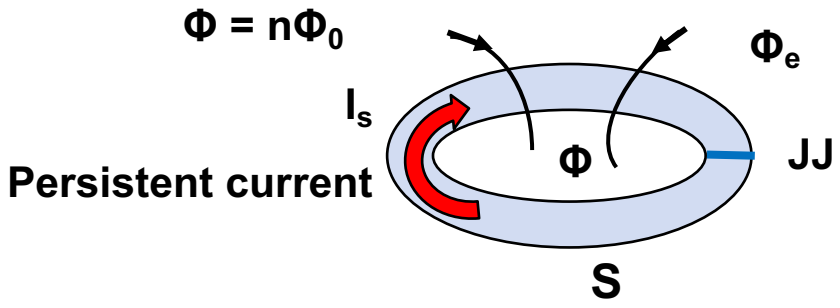
I-V Characteristics of Josephson junction



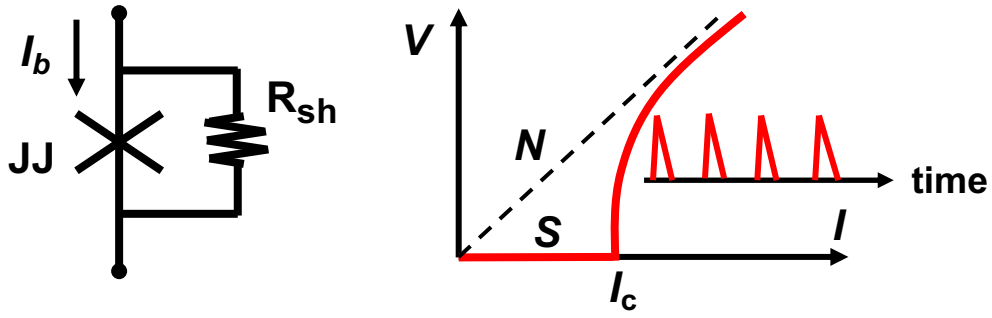
Computing with Superconductivity
Single Flux Quantum, 1985 - Present

- **Flux in a superconducting loop is quantized**
  - $\Phi = n\Phi_0$, Φ_0 - magnetic flux quantum
- **Addition of Josephson junction (JJ) in superconducting loop allows switching**
  - Generates a quantized Single Flux Quantum (SFQ) voltage pulse
- **Ultrafast switch is made from shunted JJ**
  - Voltage waveform at $I > I_c$: periodic ~ 1-ps pulses
- **Ultralow switching energy of ~10^{-19} J**
- **Single Flux Quantum (SFQ) logic/memory**
  - Proposed in 1985; thousands of circuits demonstrated
  - DC bias (early versions), synchronous / asynchronous clocking
  - Recent SFQ logic families nearly eliminate DC bias power

Josephson Junction in Superconducting Loop

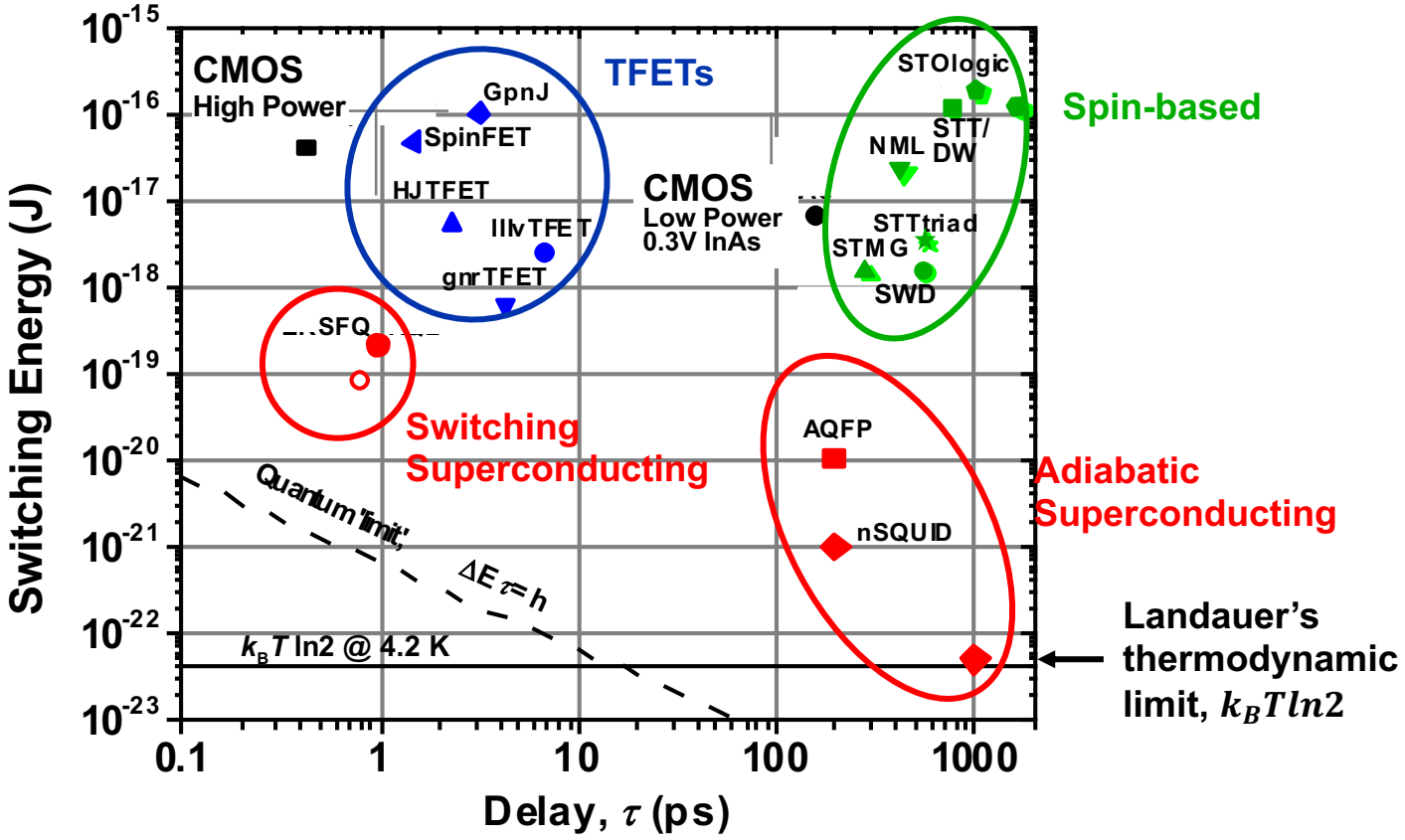


Resistively Shunted Josephson Junction (JJ)

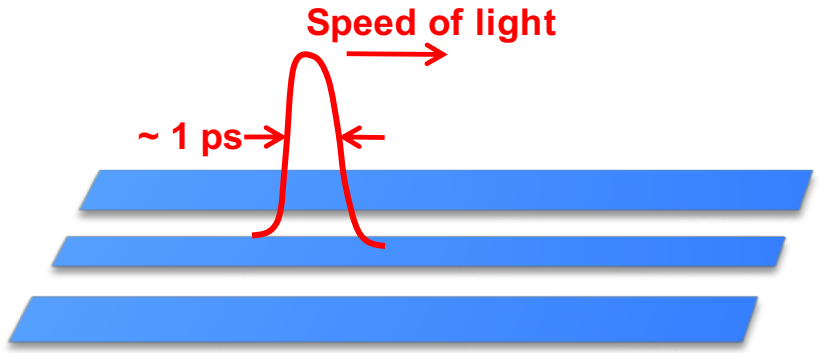


SCE as Candidate for a Beyond CMOS Technology

Ultralow Logic Energy and High Speed



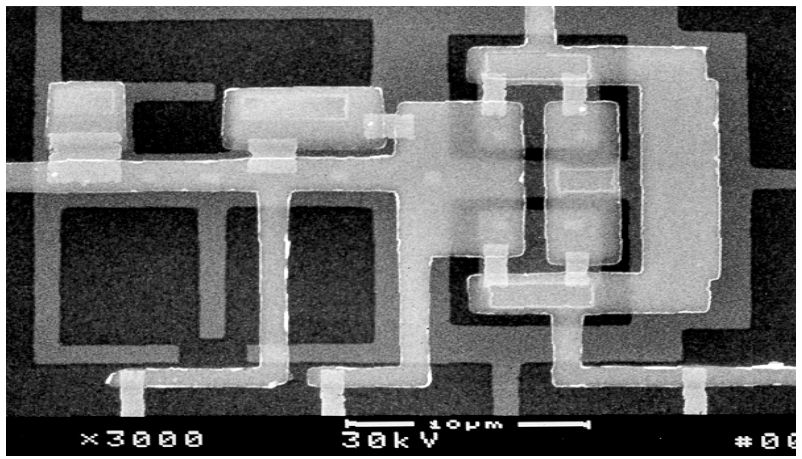
Lossless Data Transmission



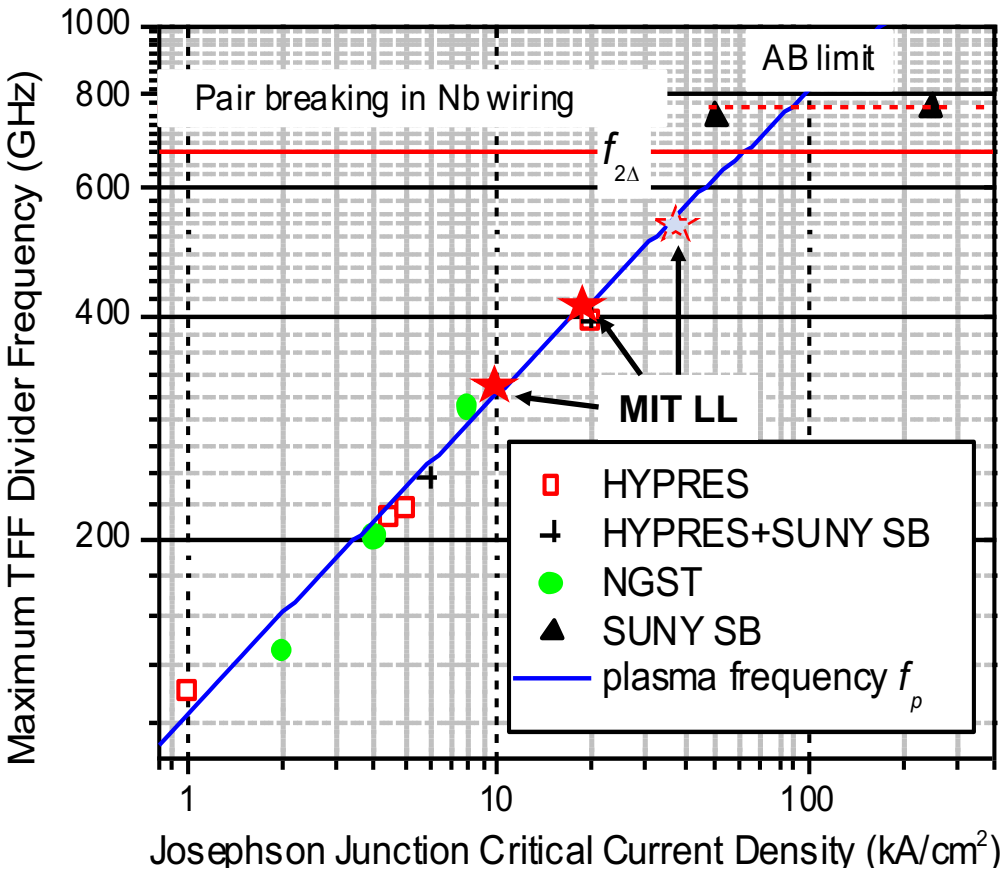
- Superconductive transmission lines provide lossless on-chip data transmission
  - Preserves ~1 ps SFQ pulses (no dispersion)
- Solution to high energy overhead of data movement in conventional processors

The Fastest Digital Technology

- Clock speed of SFQ circuits increases as $(J_c/C_s)^{1/2}$
- Early SFQ development emphasized high-speed demonstration of small-scale circuits
- 770 GHz maximum frequency of operation of SFQ static frequency dividers (T Flip-Flop) was demonstrated at Stony Brook University ~ 20 years ago



SUNY Stony Brook* 0.3-*μm*, 140 kA/cm^2, *CMP Nb Josephson fabrication process



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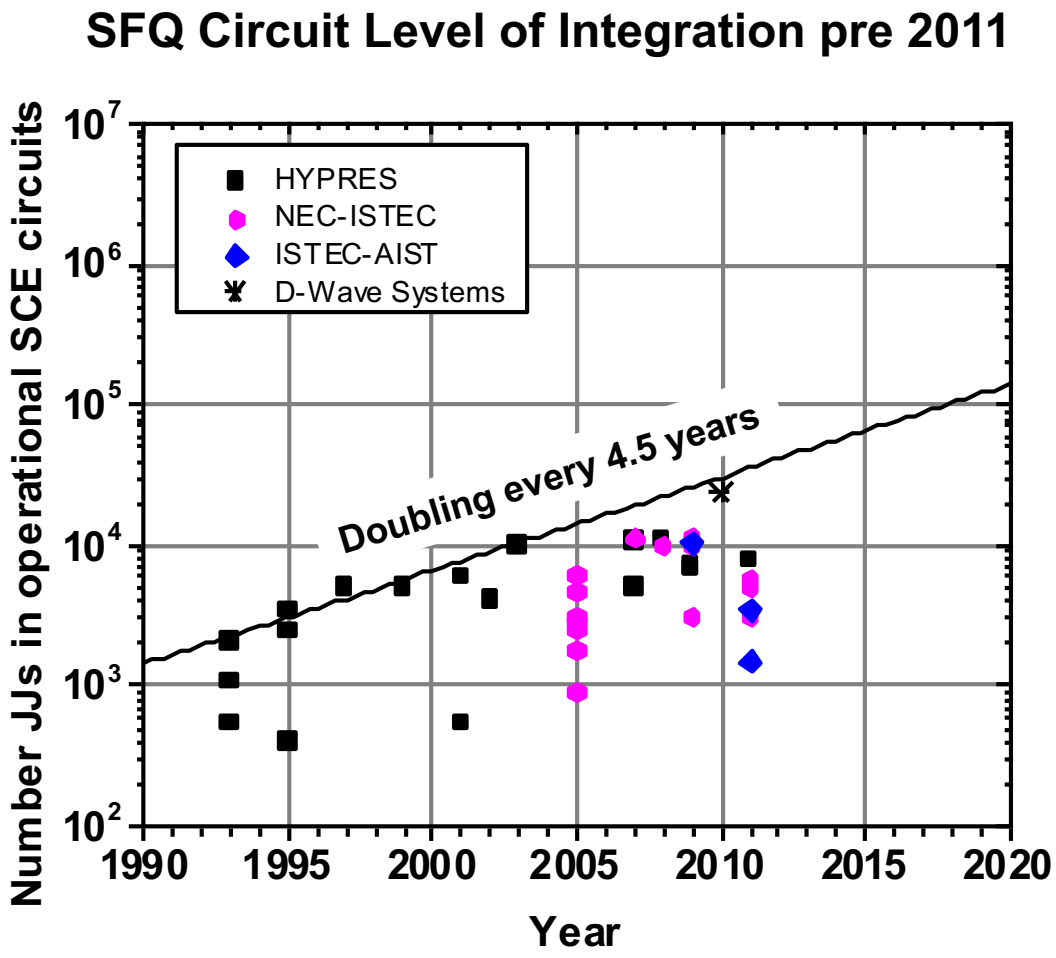
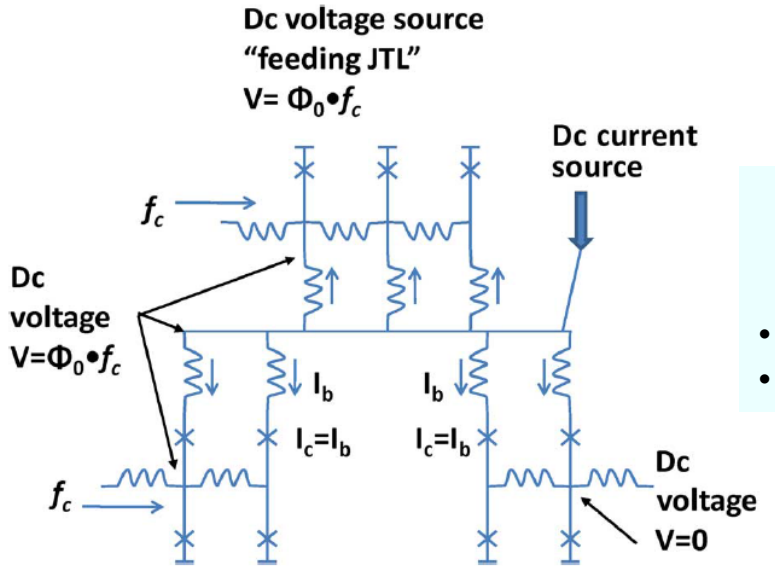
Superconducting Electronic (SCE) Circuit Trends (pre 2011)

Issues Contributing to 20,000 JJ limit

- Primary focus on high-clock-speed circuit demonstrations, not larger-scale circuits
- RSFQ circuit design limitations
  - Parallel current biasing: $I_b \propto$ number of JJs
  - Required dc bias current of over 2 A into small chips
  - Relatively large bias currents cause spurious magnetic fields that interfere with the SFQ pulse propagation
- Unsophisticated circuit design tools
- Outdated fabrication equipment



SFQ Logic Families

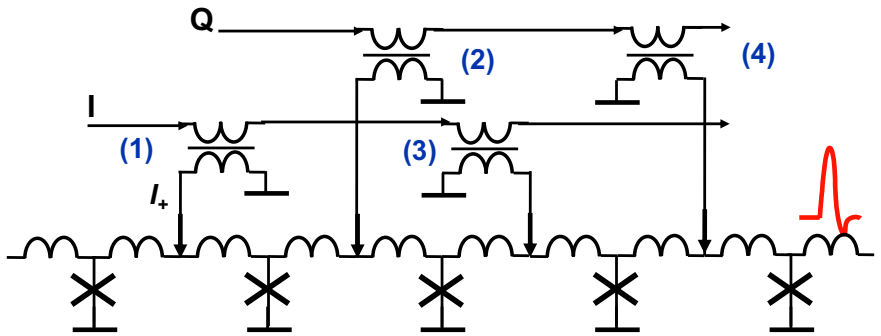


Energy-Efficient RSFQ (ERSFQ)

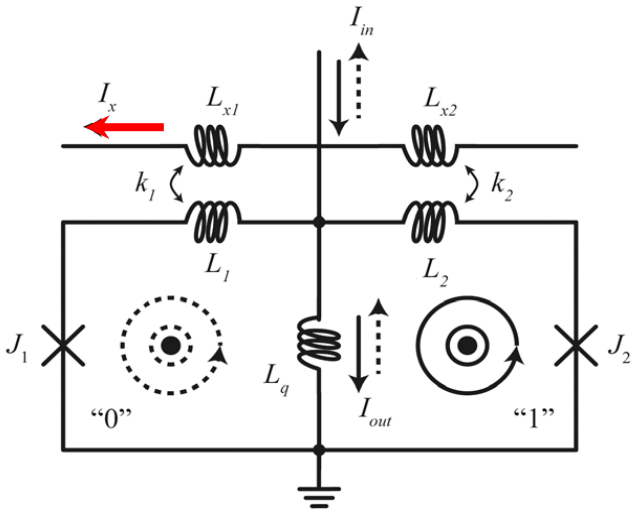
- Developed by Hypres, Inc.
- Eliminates resistor-based bias network

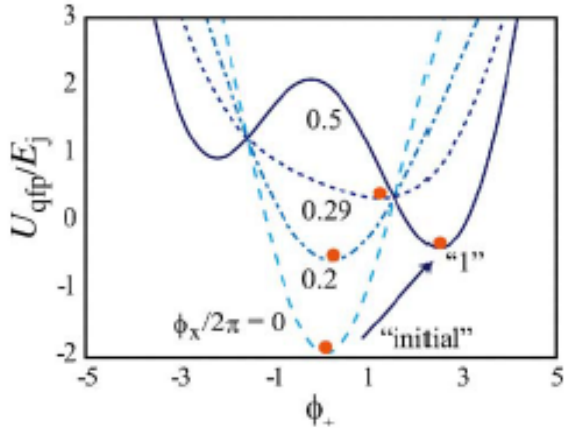
Reciprocal Quantum Logic (RQL)

- Developed by Northrop Grumman
- Based on AC biasing



Adiabatic Quantum Flux Parametron (AQFP)





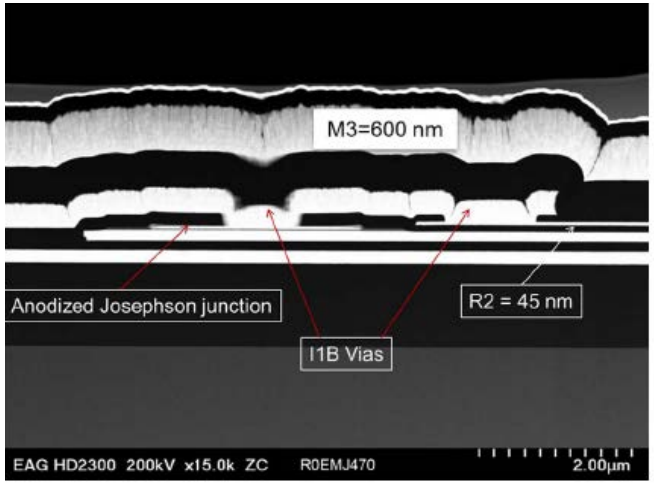
Nominal Energy per Operation for Beyond-CMOS Technologies

	Device Type	Nominal Device Energy (aJ)	Interconnect Factor	Cooling Factor	Computation Energy per Operation (aJ)	
Commercial State-of-the-Art	HP CMOS	18	100x	1.5x	2700	← Today
Advanced Semiconductor Technologies	LP CMOS 0.3-V InAs	3.3	100x	1.5x	500	
	Tunneling FETs	1.5	100x	1.5x	220	← ~10x improvement
Superconducting Technologies	Switching SFQ @ 4 K	0.1	1x	500x	50	
	AQFP @ 4 K	0.01	1x	500x	5	← ~500x improvement
	Nearly reversible @ 4 K	0.001	1x	500x	0.5	

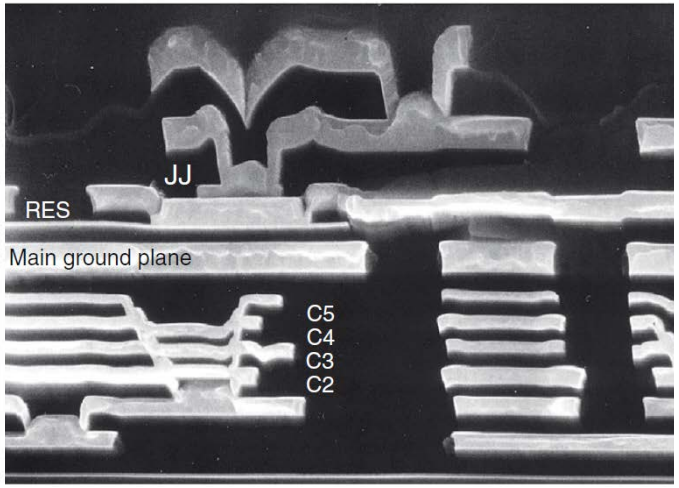
Superconducting electronics offers orders of magnitude reduction in energy consumption, even with requirement to cool to 4 K temperature

State-of-the-Art Superconducting Circuit Fabrication

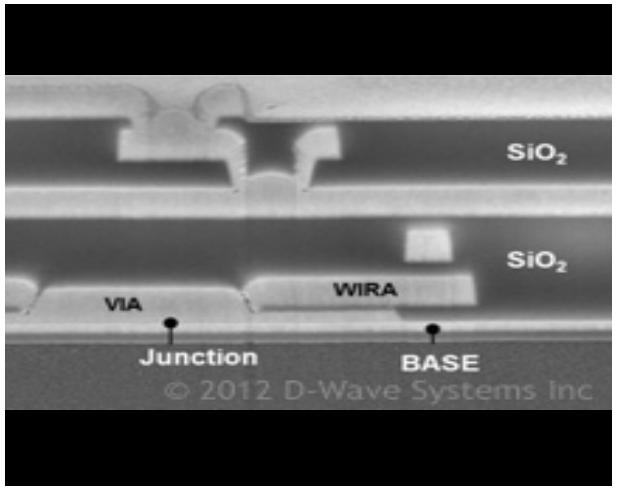
HYPRES 4-Layer Process (USA)



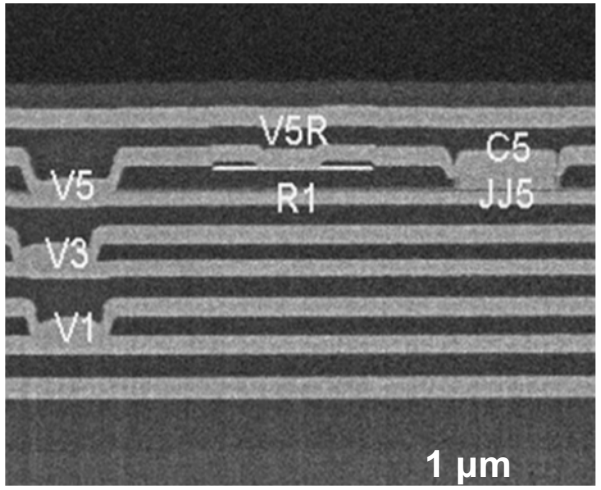
AIST 10-Nb-Layer (Japan)



D-Wave Systems 6-Nb-Layer



MIT LL 8-Nb-Layer Process

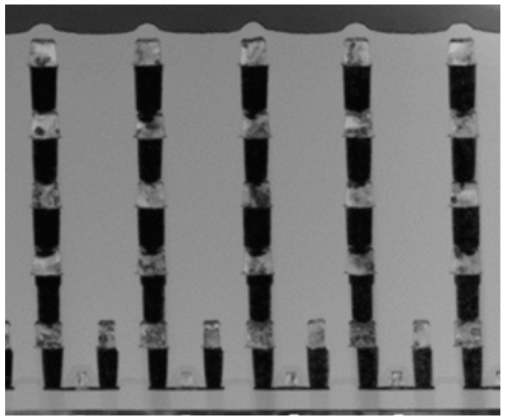


Wafer size	**150 mm**	**75 mm**	**200 mm**	**200 mm**
Number of Nb layers	**4**	**9 and 10**	**6**	**8 and 9**
Planarization	**No planarization**	**Partial planarization**	**Full planarization**	**Full planarization**
Min wiring feature size	**~ 1 µm**	**~ 1 µm**	**250 nm**	**350 nm**
Min JJ size	**~ 1.5 µm**	**~ 1.2 µm**	**600 nm**	**700 nm**
Integration scale	**11k JJs**	**80k JJs**	**128k JJs**	**810k JJs**

***AIST: National Institute of Advanced Industrial Science and Technology, Japan**

Contrast to 90nm FDSOI CMOS Fabrication Process

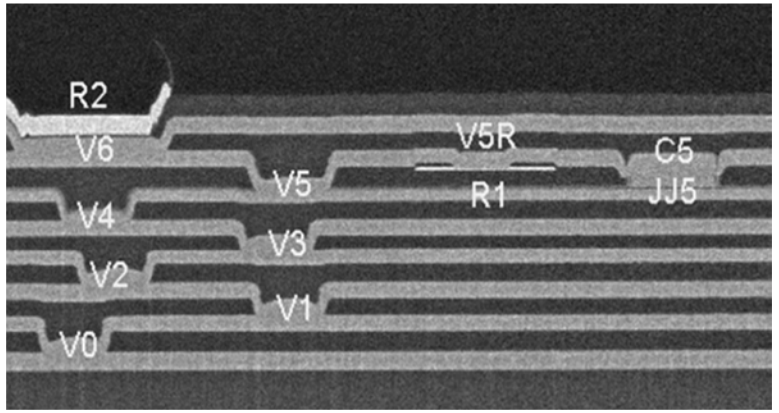
90-nm FDSOI CMOS Cross Section



Passive Wiring Layers
Interconnect, vias, inductors

Active Layers
Transistors, capacitors, resistors

Superconducting Electronics Cross Section



Active Layers
JJs, resistors

Passive Wiring Layers
interconnect, vias, inductors

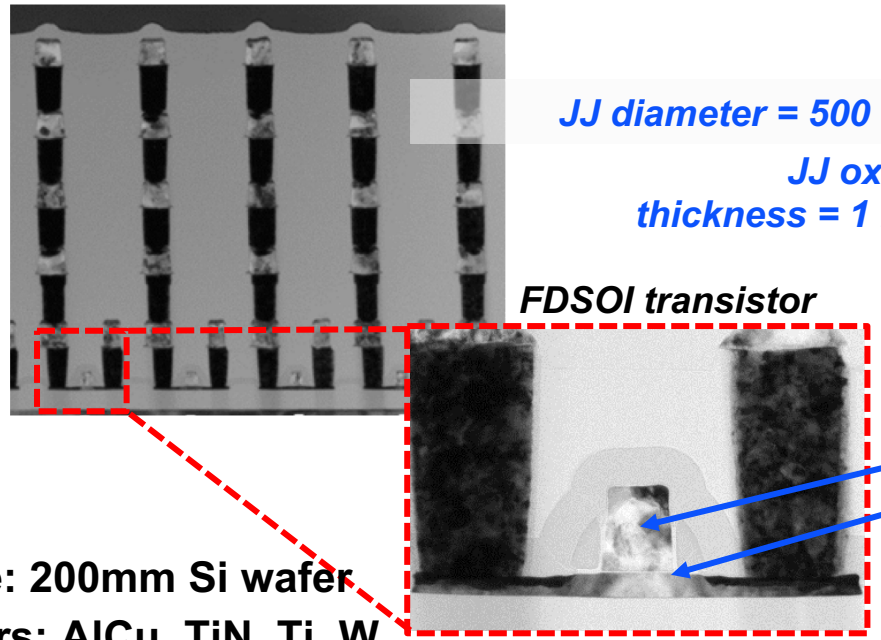
- **CMOS is tolerant of process variability: >10%**
- **Planarization of metal layers is primarily done for patterning (DOF)**
- **Thickness between metals can vary up to 10% across wafer with minimal electrical impact (R, C)**

- **SFQ allowed variability is much less**
  - **Active devices: < 1%**
  - **Inductors (wires): < 5%**
  - **Dielectric thickness: < 10%**
- **Critical parameters: device area, tunnel barrier uniformity**

SFQ circuit performance is much more dependent on process control than CMOS circuits

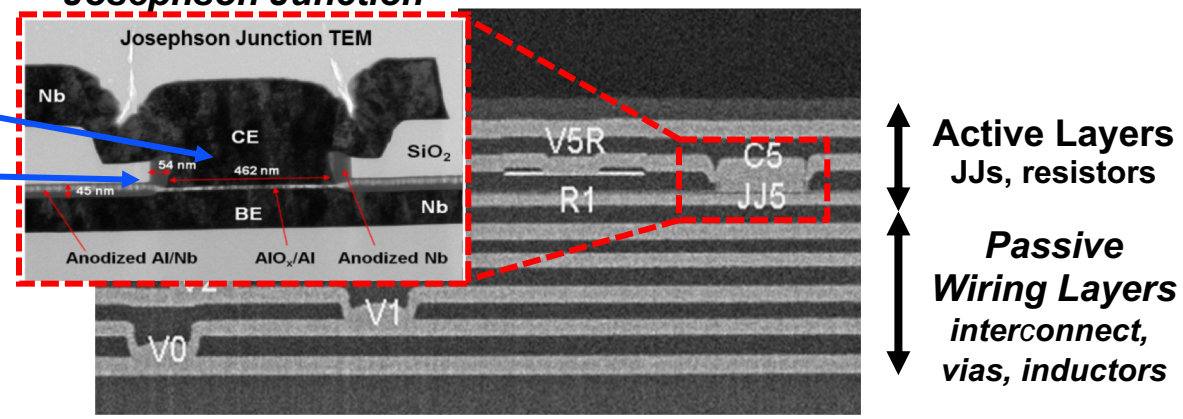
Contrast to 90nm FDSOI CMOS Fabrication Process

90-nm FDSOI CMOS Cross Section



- Substrate: 200mm Si wafer
- Wire layers: AlCu, TiN, Ti, W
- Inter-metal dielectric: PECVD SiO_2 at 400°C
- Device active layers: HfO_2, Si_3N_4, SiO_xN_y, polysilicon, $CoSi_2$

Superconducting Electronics Cross Section

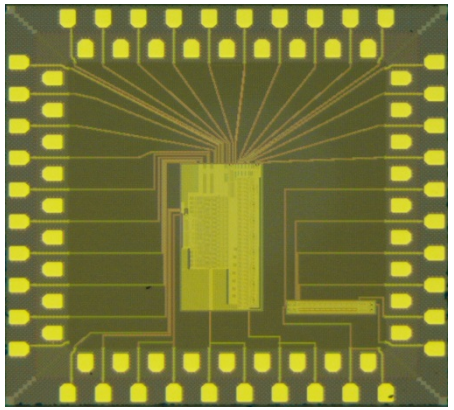


- Substrate: 200mm Si wafer
- Wire layers: Nb, MoN_x, $NbTiN_x$
- Inter-metal dielectric: PECVD SiO_2 at 150°C
- Device active layers: Nb/AlO_x/Al/Nb
- Resistors: Ti/Mo, Ti/MoN_x

Both SFQ and CMOS active devices rely on well-controlled, sub-nm-scale oxide layers

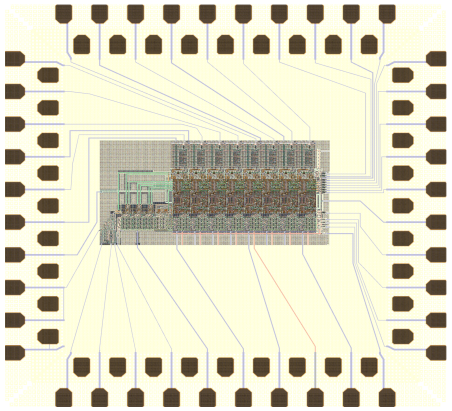
Northrop Grumman and Hypres Circuit Designs Fabricated in MIT LL Process (IARPA C3 Program)

Hypres Designs



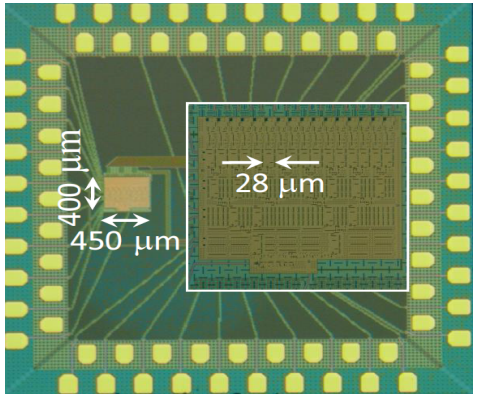
ERSFQ 32-bit slice of Register with Decoder

- **Access time: 100 ps**



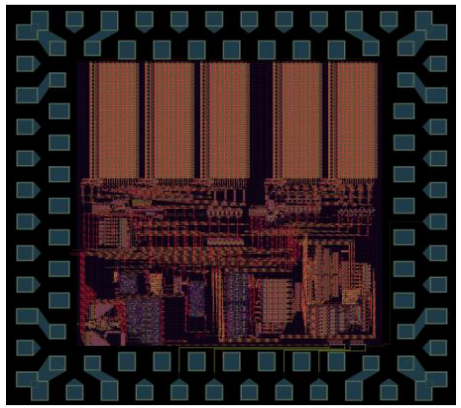
ERSFQ 8-bit ALU

- **JJ count: 7200**
- **Clock: 10 GHz**



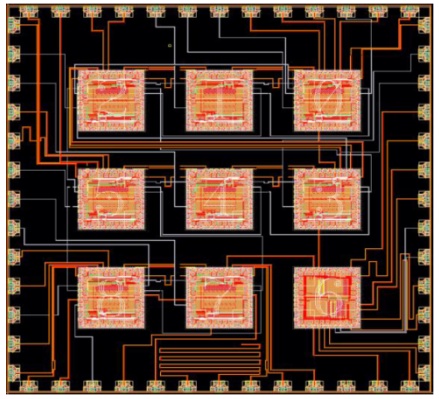
ERSFQ 4-to-16 bit Decoder

- **Delay: ~ 30 ps**
- **Energy: ~40 aJ /clock**
- **Clock: 13 GHz**



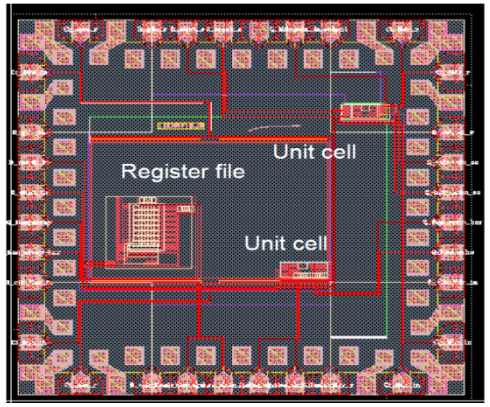
RQL 8-bit CPU

- **Gates: ~5600**
- **JJ count: ~ 25,000**



9-chip Multi-Chip Module
32 mm x 32 mm

Northrop Grumman Designs



RQL Register

- **Gates: 222**
- **JJ count: ~ 2,500**
- **Tested @: 4.7 GHz**

VLSI Integration Demonstrated at MIT-LL

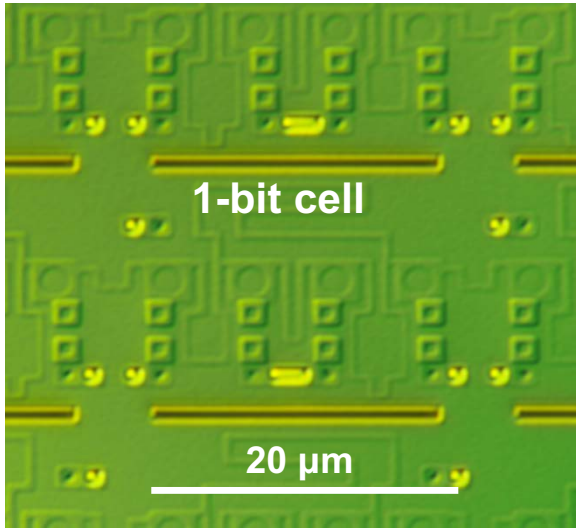
World Record in JJ Count

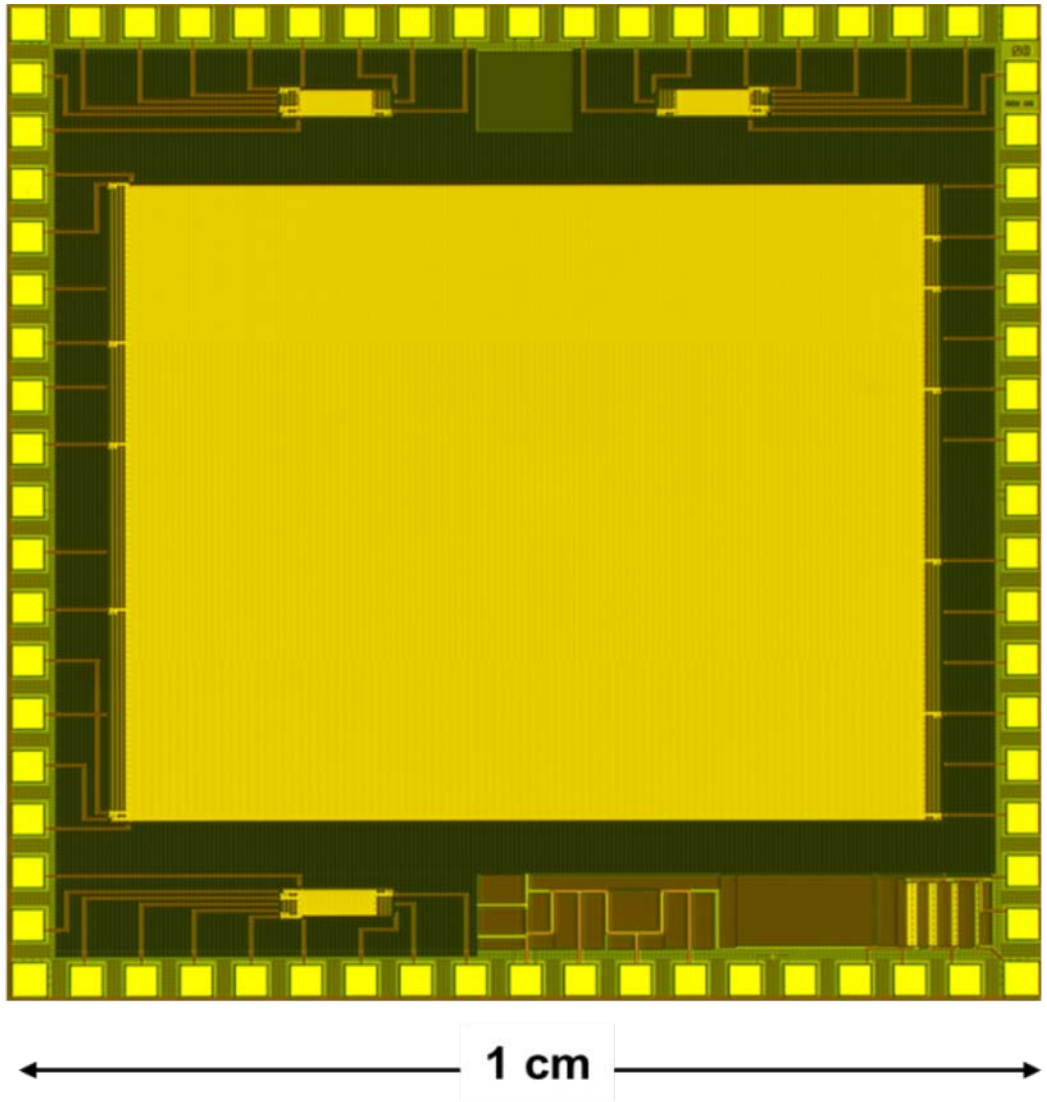
- **AC-biased shift register: 202,000 bits**
- **JJ count: 810,000+ (World Record)**
- **Integration scale: ≈ Intel's Pentium, 0.8-μm process, 3.1M transistors on 294 mm² chip**
- **100x increase in integration scale during four years**

- **Cell size:**

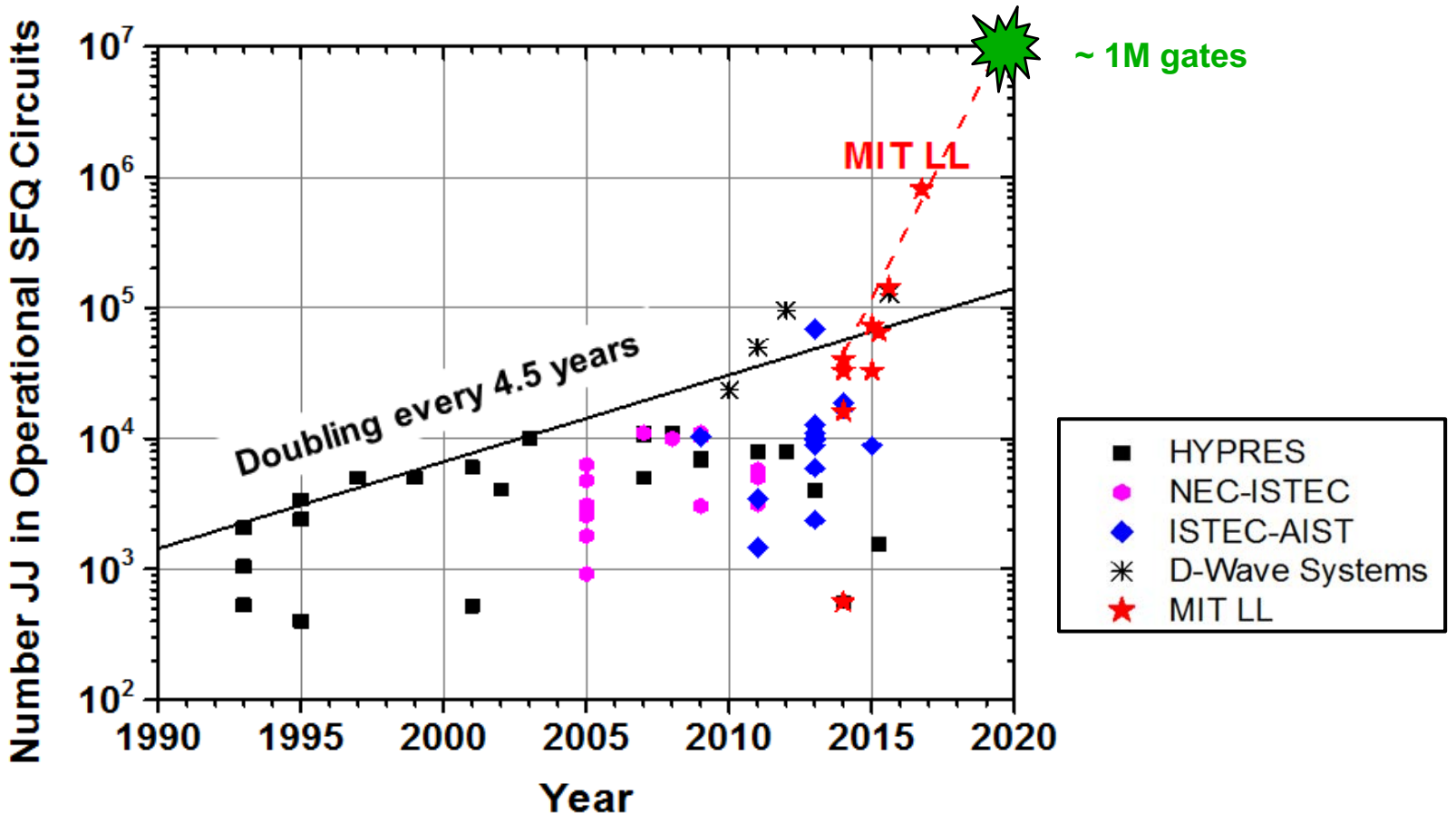
  20 μm x 15 μm
- **JJ density:**

  $1.33 \cdot 10^6$ JJ/cm²





Superconducting Electronics Scaling Trends



Superconducting electronics can now be fabricated at the very large scale integration (VLSI), and the next challenge is demonstrating application-relevant impact

Outline

- Introduction to Superconducting Electronics
- Technology Development for Digital Computing
- Additional Applications

Superconducting Electronics Application Domains

Digital Electronics

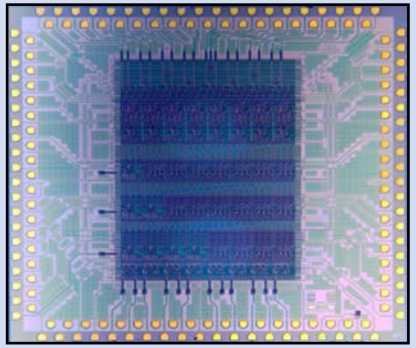


Image: HYPRES

- Digital circuits have been pursued since the early 1950s
- Increasing interest in both high-performance computing and control circuit applications
- Poised for significant progress in the next 5 – 10 years

RF Electronics

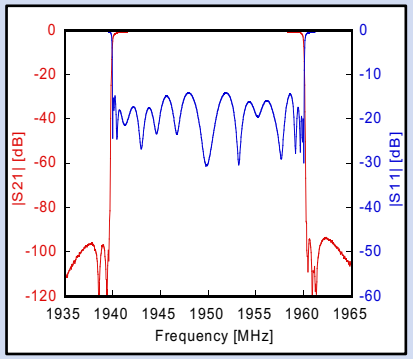


Image: IEEE Trans MTT (2000): 2519

- Extremely small RF electrical resistance enables very high quality factor components
- Used in particle accelerators and free electron lasers
- Maturation of fabrication processes can be leveraged to expand use in RF applications

Quantum Computing

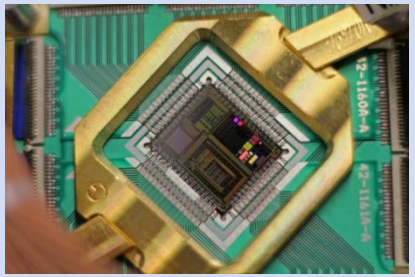


Image: Google

- Superconducting quantum bits (qubits) are a leading candidate for quantum computation (QC)
- Dominant QC approach pursued by commercial companies
- Superconducting electronics are also being pursued for qubit control and readout

Detectors and Sensors

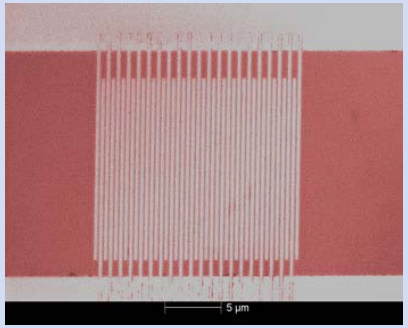
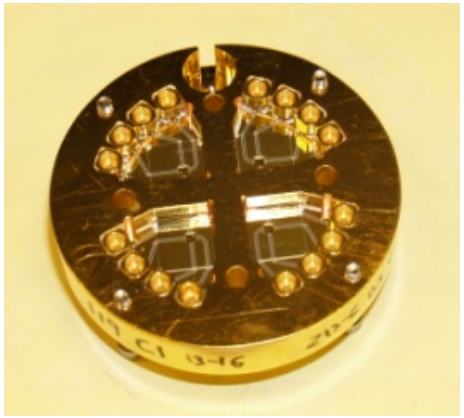


Image: NIST

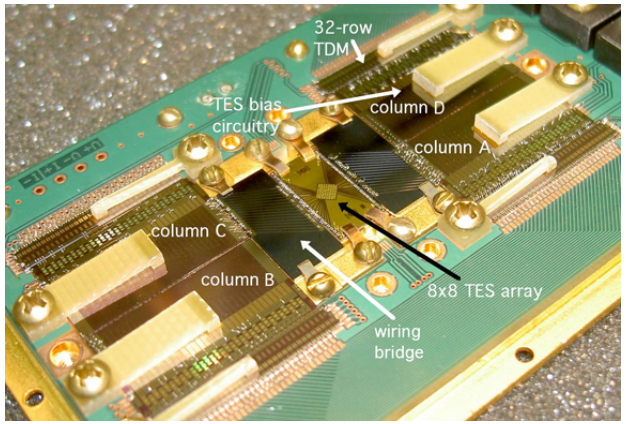
- Used in scientific, astronomy and metrology applications
- Voltage standard and high-sensitivity magnetometers
- Broadband optical detectors and unique energy resolution in the single photon domain

Control Electronics for Superconducting Devices

Superconducting Detector Arrays



MIT Lincoln Laboratory
Existing 4x4 element array of Superconducting Nanowire Single Photon Detectors (SNSPDs)

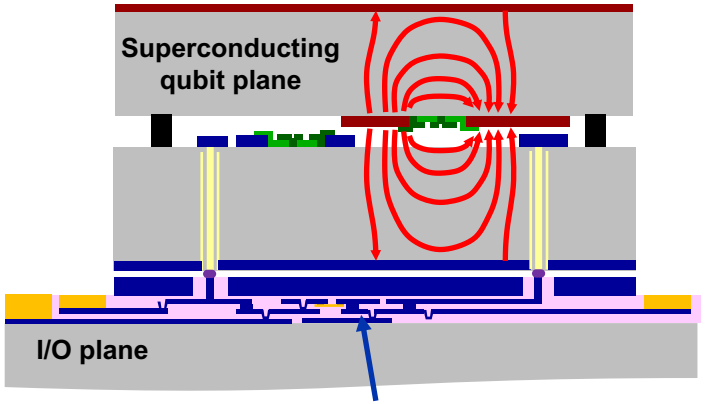


NASA Goddard & NIST
Existing 8x8 pixel Transition Edge Sensor (TES) array

MIT LL superconducting electronics fabrication paired with existing circuit design could enable multi-kilopixel detector arrays

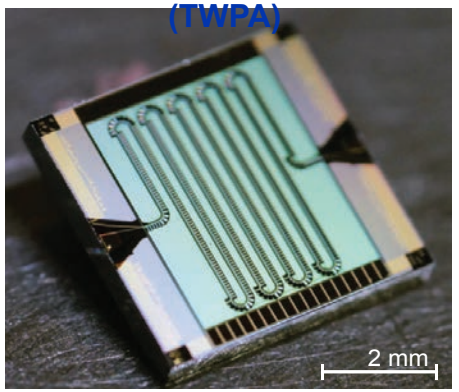
IARPA Quantum Enhanced Optimization (QEO) and Logical Qubit (LogiQ) Programs

MIT Lincoln Laboratory
3D Integrated Superconducting Qubit Platform



MIT LL multi-layer superconducting electronics is critical to achieving the required I/O density for quantum annealing systems

MIT LL & UC Berkeley
Traveling-Wave Parametric Amplifier (TWPA)

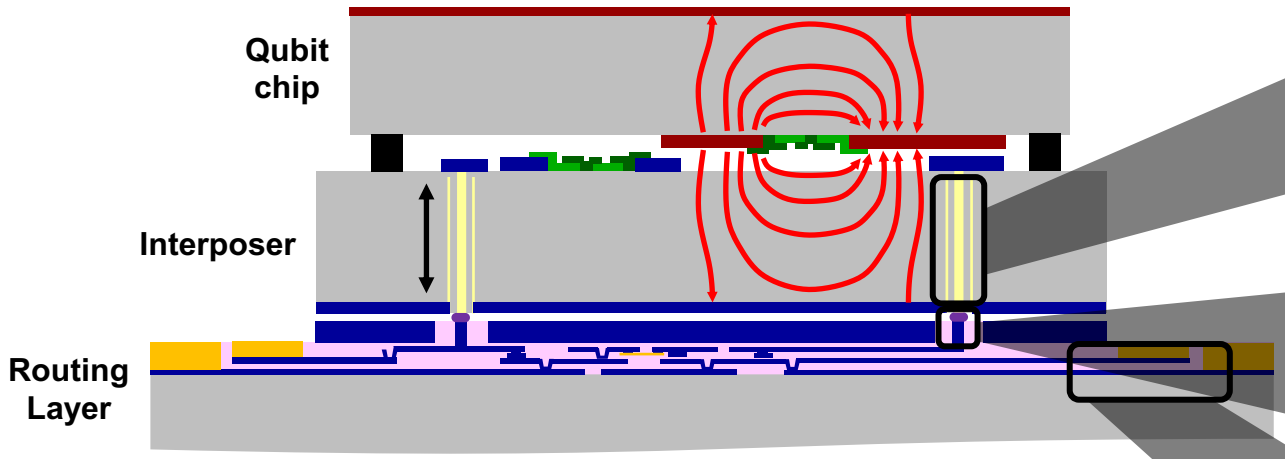


MIT LL superconducting electronics fabrication process enables multi-GHz bandwidth, near-quantum-limited amplification

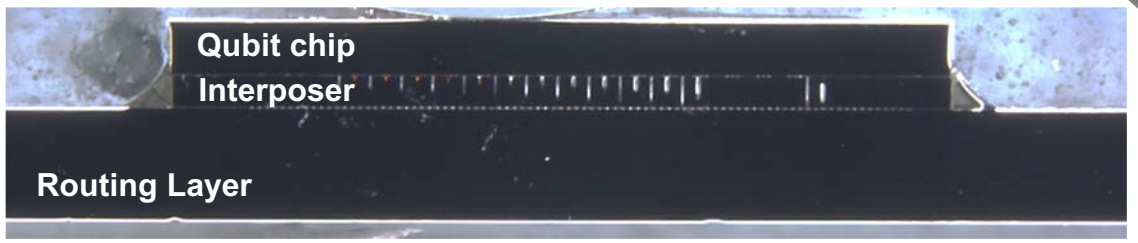
Advances in superconductor electronics at MIT Lincoln Laboratory are enabling unique quantum systems

Technologies for 3D Integration of Superconducting Qubits

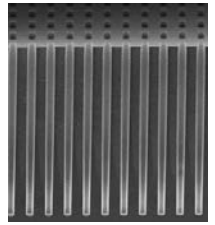
3D Superconducting Chip Stack Diagram



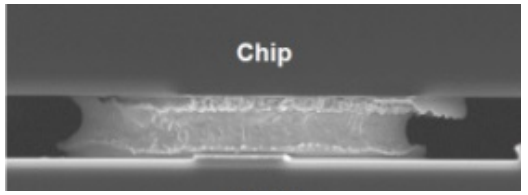
3D Superconducting Chip Stack Image



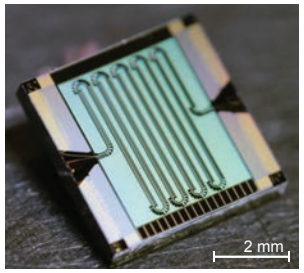
Through-substrate vias (TSVs)



Superconducting bumps



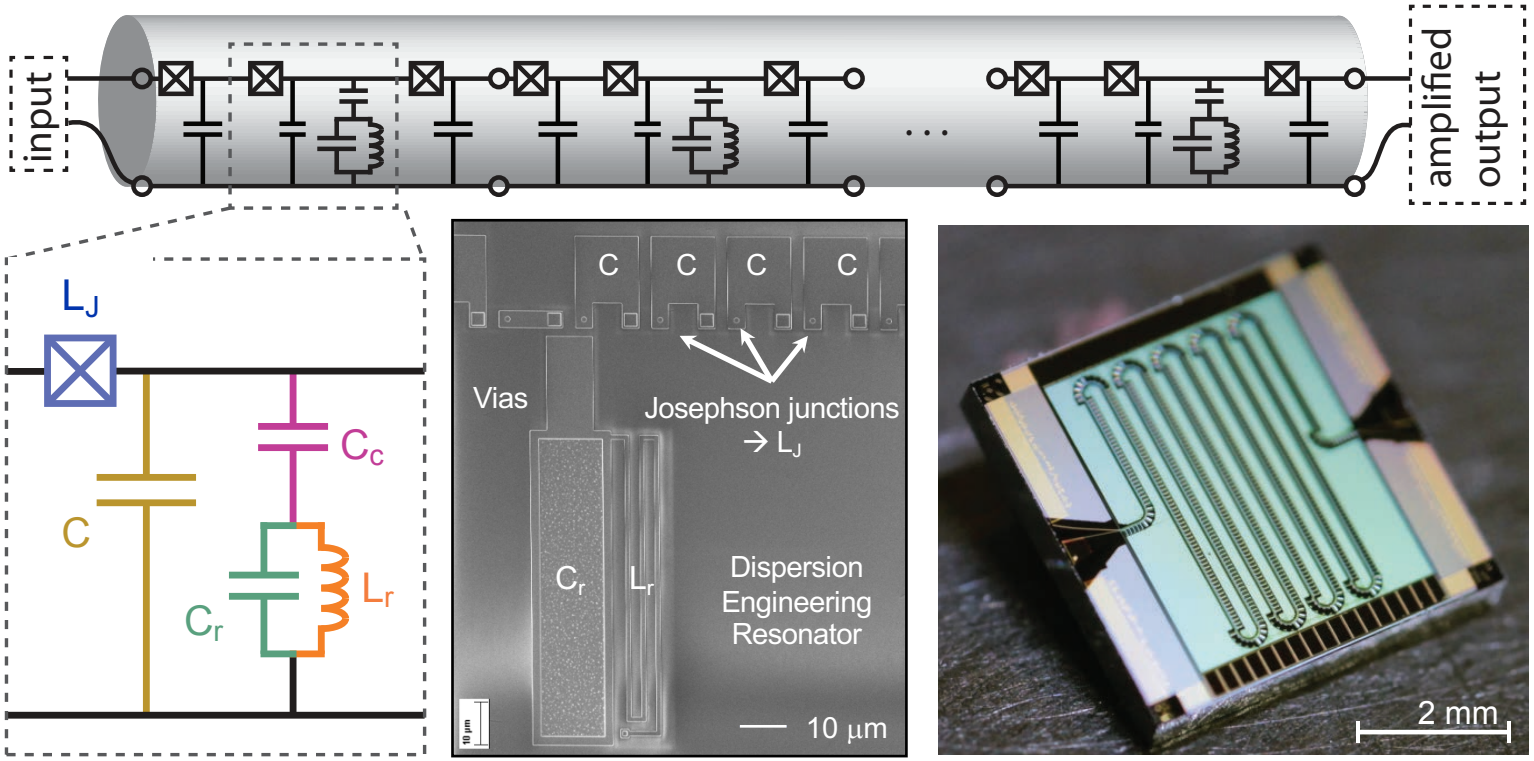
Traveling Wave Parametric Amplifiers (TWPAs)



3D integration approaches are being developed to support required connectivity to qubits while maintaining high coherence

D. Rosenberg et al., npj Quantum Information (2017).

Traveling-wave Parametric Amplifier (TWPA)



- **Narrow-band Josephson parametric amplifiers first demonstrated in late 1980s**
- **Traveling-wave parametric amplifiers offer broadband, quantum-limited noise performance**
  - **>4 GHz bandwidth**
  - **400 mK noise temperature**
- **Leverages unique multi-layer superconducting Nb fabrication process at MIT Lincoln Laboratory**

TWPA devices fabricated at MIT Lincoln Laboratory are supporting R&D at many universities, companies and Government laboratories

C. Macklin et al., Science 350, 307 (2015)

Summary

- Significant increase in interest in superconducting electronics over the past decade
  - Classical computation
  - Control electronics for cryogenic devices, particularly detectors and sensors
  - Quantum computing
- Rapid advances in Nb trilayer fabrication processes
- Future development of superconducting electronic systems will rely on advances in many technologies beyond just superconducting integrated circuits
  - Cryogenic systems
  - Cryogenic packaging and interconnects
  - Superconducting design and simulation tools
  - New architectures, algorithms and software